Acta Technica 62 (2017), No. 4A, 255–258

Research and implementation of gauss noise digital fm algorithm based on fpga

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Abstract. In order to solve the disadvantages of the traditional way in producing noise FM signals, such as, poor stability, low control accuracy and failing to achieving a real-time processing, in this paper, a Gauss noise digital FM algorithm based on FPGA was proposed, where the generation of Gauss white noise random variables is achieved by the additivity of a normal distribution, FM function is realized by DDS, the resulting signal coherence and controllability are very stringent, and the whole system is debugged and completed on FPGA. Test results show that this system has the advantages of small computation, high speed, on-line upgrading and configurable, and the generated noise digital FM signal is not affected by the external environment.

Key words. Fpga, noise frequency modulation signal, configurable, dds.

1. Introduction

Relatively simple analog or semi digital methods are commonly used to generate noisy FM signals [1-2]. This kind of noise FM signal has the disadvantages of poor stability, low control accuracy, great impact on the external environment, and failing to achieving a real-time processing, therefore, the application has been greatly limited [3-4]. In order to solve the problem, this paper proposed a Gauss noise digital FM algorithm based on FPGA. In this algorithm, the noise FM signal is mainly generated by DDS soft core and implemented on FPGA, and the noise FM signal produced by this system has the advantages of on-line updating, real-time processing and full digitalization.

[1]Acknowledgment - This work is supported by the Science Foundation of Jiujiang University (Grant Nos. 2015LGYB01,2016KJ001,2016KJ003).

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2. Generating Principle of Digital Noise Frequency Modulation Signal

Text of the second section. The time domain of the noise FM signal can be expressed as:

$$u(t) = A_0 \cos(2\pi f_0 t + K_f \int_0^t \nu(t)dt + \phi_0) \quad (1)$$

In Formula (1), A_0 is an amplitude, K_f is a FM index, φ_0 is a carrier phase, ν(t) and is the generalized stationary random process with a zero mean [5] .
Set $_d$ as an effective frequency and as an instantaneous frequency deviation, K_f = $_d$, = - $_c$, then the actual power spectrum of the noise FM signal can be expressed as:

In Formula (2), P_0 is an actual total power, P_0=1/2Am^2. The half power spectral bandwidth of a noise FM signal isWhen one of the two parameters which refers to the FM index $K_f$and the root mean square of noise variance is given, another parameter can be found, and the bandwidth of the half power spectrum is also guaranteed.

3. Overall Design of System Hardware

Which mainly includes power supply configuration circuit module, clock distribution module, DAC module and FPGA module, where FPGA module is the core control module of the system which can develop the FPGA chip by Quartus II. The power supply module mainly provides 3.3V and 5V voltage to the FPGA chip, which are mainly achieved through the switching power supply chip and linear power chip and other chips; the clock allocation module provides stable clock signals for FPGA, DAC, and PCI9054.

4. System Structure Design

4.1. The occurrence of uniform random signals

The Tausworthe algorithm was used to quickly realize uniform pseudo-random sequences. The specific structure diagram is shown in Figure1.

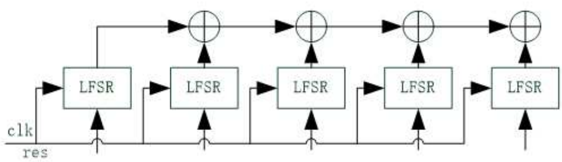


Fig. 1. Hardware structure diagram of uniform random signal generating unit

4.2. Address generation module

The module mainly performs orthogonal transformation of the input uniform random variables, at the same time, output four independent addresses, p, q, r, s, with the length of n_2. This provides not only the read address before transformation but also the write address after translation[6].

4.3. Orthogonal transform module

After normalizing the Gauss variables to generate the module, the variables are the standard normalized Gauss random variables. The main function of the orthogonal transform module is to minimize the association between this variable and the source variable before transformation. 1024 normalized Gauss random variables are stored on the ROM, an uniform random address will read and write dual port RAM when the system is running, which allows us to complete the output of two normalized random variables. Y can be obtained from a random number X by an orthogonal transformation module $Y=A_iX$ i=1 2 3 4 . In calculations, the orthogonal transformation matrices A_1, A_2, A_3, and A_4 are used sequentially.

4.4. Schematic diagram of DDS hardware structure

DDS is mainly implemented by sampling and computing techniques, which can realize the sinusoidal signal an adjustable frequency. The schematic diagram of the hardware structure is shown in Figure2.

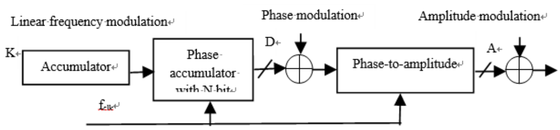


Fig. 2. Schematic diagram of dds hardware structure

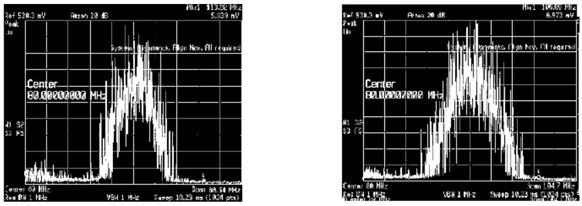
5. Test Results and Conclusions

The system obtained 1×10^5 random variables through the software Modelsim and analyzed these sequences by MATLAB. The two parameters, mean and variance, are calculated at the same time, the mean is 0.0016 and the variance is 1.001, which are essentially equal to the theoretical value of the normalized Gauss noise.

Test the signal with a spectrum analyzer, which can prove that the noise FM signal output by this system is in line with expectations. The specific test results are shown in Figure3.

In Figure 3(a), $K_f=16.138\times10^6$ $A_0=1$??$\omega_c=80\times10^6$, the bandwidth is 80.54MHz, while in Figure 3(b), $K_f=22.369\times10^6$ $A_0=1$ $\omega_c=80\times10^6$ and the bandwidth is 104.7MHz.

In this paper, a Gauss noise digital FM algorithm based on FPGA was proposed,



(a) $\Delta w_{0.5}=40.27$ MHz (b) $\Delta w_{0.5}=52.35$ MHz

Fig. 3. Frequency spectrum of noise fm signal

the article not only analyzed the generating principle of noise frequency modulation signal, but also discussed the producing process of Gauss noise digital FM signal in detail, at the same time, the hardware implementation was also carried out. Not only the simulation analysis, but also the actual test have been performed. Tests and results show that this system has the advantages of small computation, high speed and configurable.

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Received November 16, 2016